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STL NEMS in Silicon – Status and Limitations

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Abstract

Sidewall transfer lithography (STL) is a well-established method of pattern transfer that allows resolution to be reduced below the wavelength of light using low-cost equipment and was originally developed for fabricating short gates in field effect transistors. A multistep patterning process is involved. Optical lithography is first used to create microscale features in resist, which are transferred into a substrate using reactive ion etching (RIE). The resulting mesas are conformally coated with an additional layer of material, often an oxide. The horizontal surfaces of this layer are removed by further RIE, leaving the vertical sidewall surfaces to act as a mask for subsequent etching. The width of the sidewall features is then determined by the coating thickness and can be nanoscale. However, this width must be uniform and sidewall features must correspond to perimeters of polygonal shapes. Careful attention must therefore be given to layout and the partitioning of features of different sizes between mask layers. When combined with additional conventional lithography, deep reactive ion etching, and sacrificial layer processing steps, STL allows the mass parallel fabrication of movable nanoscale elements and is therefore intrinsically suitable for foundry-scale production of nanoelectron-mechanical systems (NEMS). Design strategies, developments and limitations in processing, and applications in silicon NEMS devices and materials will be described.